

### **ABSTRACT OF THE DISCLOSURE**

The present invention discloses a layout method of a comparator array of a flash type analog to digital converting circuit. The flash type analog to digital converting circuit includes a reference voltage for generating  $2^n$  voltages and being arranged to be folded; a comparator array including  $(2^n-1)$  comparators for comparing voltage differences between the respective  $2^n$  number of voltages and an analog input signal to generate a digital signal having  $(2^n-1)$  thermometer codes; and an encoder for encoding the digital signal having  $(2^n-1)$  thermometer codes to generate an n-bit digital signal. The layout method of the flash type analog to digital converting circuit comprises arranging the comparators such that the comparators of  $(2^n-1)^{\text{th}}$  comparator to  $(2^n/2)^{\text{th}}$  comparator are arranged in order and the comparators of  $(2^n/2-1)^{\text{th}}$  comparator to a first comparator are arranged in reverse fashion between the comparators of the  $(2^n-1)^{\text{th}}$  comparator to the  $(2^n/2)^{\text{th}}$  comparator; and arranging the comparators such that the neighboring comparators adjacent to the respective  $(2^n-1)$  number of comparators transit to the same state when the  $(2^n-1)^{\text{th}}$  comparator to the  $(2^n/2)^{\text{th}}$  comparator transit to different states respectively. Therefore, increasing of an offset voltage due to the effects of the neighboring comparators is prevented without increasing a layout area size.

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